a replica circuit of said adjusted circuit in which a second bias current flows, a value of said second bias current being substantially equal to that of said first bias current;

an evaluation circuit configured to repeat a cycle of processing, said cycle of processing including:

resetting an output thereof;

obtaining a difference between first and second voltages at given times, said first voltage being one at an output of said replica circuit at a time when a first time interval has elapsed after a given voltage having been step-inputted to said replica circuit, said second value being one at said output of said replica circuit at a time when a second time interval has elapsed after a voltage equal to said given voltage having been step-inputted to said replica circuit, said second time interval being different from said first time interval; and

successively summing said differences;

a comparator circuit for comparing a value obtained by said successively summing with a reference value; and

a bias adjustment circuit for changing said second bias current according to a comparison result of said comparator circuit at every said given times.

2. (Amended) The semiconductor integrated circuit of claim 1, wherein said evaluation circuit comprises:

a subtraction/integration circuit integrating, as said successively summing, each difference between said first voltage and said second voltage; and

a control circuit;

wherein said control circuit is configured to repeat the steps of:

(1) resetting said subtraction/integration circuit [to be reset];

(2) repeating part of said cycle of processing at said given times, said part of said cycle of processing including:

resetting said replica circuit;

next step-inputting said given voltage to said replica circuit;

next providing said first voltage to said subtraction/integration circuit after or till said first time interval has elapsed from said step-inputting;

next resetting said replica circuit;

next step-inputting said voltage equal to said given voltage to said replica circuit; and

next providing said second voltage to said subtraction/integration circuit after or till said second time interval has elapsed from said previous step-inputting.

3. (Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step up said second bias current in response to judgment that a value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation of said bias adjustment circuit in response to judgment that said value obtained by said successively summing is smaller than said reference value.

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4. (Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and

wherein said control circuit is configured to cease operation of said bias adjustment circuit in response to judgment that said value obtained by said successively summing is larger than said reference value.

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5. (Amended) The semiconductor integrated circuit of claim 2,

wherein said bias adjustment circuit is configured to step down said second bias current in response to judgment that a value obtained by said successively summing is smaller than said reference value by said comparator circuit, and step up said second bias current in response to judgment that said value obtained by said successively summing is larger than said reference value by said comparator circuit,

wherein said control circuit is configured to cease operation of said bias adjustment circuit in a case where an absolute value of a difference between said value obtained by said successively summing and said reference value is smaller than a given value.

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6. (Amended) The semiconductor integrated circuit of claim 3,

wherein said replica circuit has an inverting output and a non-inverting output,

wherein said subtraction/integration circuit comprises:

an operational amplifier circuit having an inverting input, a non-inverting input, an inverting output and a non-inverting output;

a first integrating capacitor connected between said inverting input and non-inverting output of said operational amplifier circuit;

a second integrating capacitor connected between said non-inverting input and inverting output of said operational amplifier circuit;

a reset switching circuit for resetting electric charges on said first and second integrating capacitors;

first and second sampling capacitors; and

a switching circuit for selectively charging said first and second sampling capacitors or said second and first sampling capacitors by said inverting output and non-inverting output, respectively, of said replica circuit, and thereafter transferring electric charges on said first and second sampling capacitors to said first and second integrating capacitors, respectively.

REMARKS

The Office Action dated March 27, 2002 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-6 have been amended. The amendments made address matters of form and are cosmetic in nature, and are not made to overcome the cited prior art. No new matter has been added or amendments made which narrow the scope of any elements of any